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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wang et al.

Attorney Docket No.: NOVL085/
NVLS-2875

Application No.: 10/785,235

Examiner: UNASSIGNED

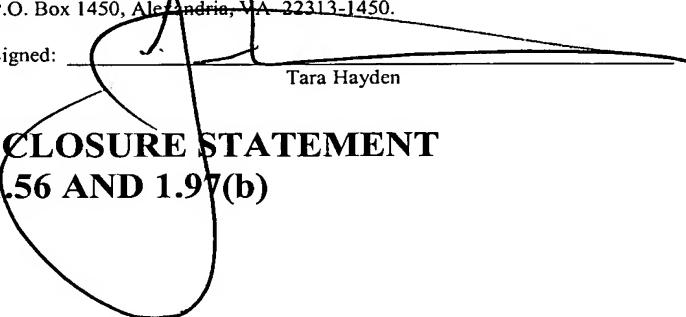
Filed: February 23, 2004

Group: 2812

Title: PLASMA DETEMPLATING AND
SILANOL CAPPING OF POROUS
DIELECTRIC FILMS

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on June 23, 2005 in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: 

Tara Hayden

**INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NOVLP085).

Respectfully submitted,
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Form 1449 (Modified)	Atty Docket No. NOVL085/NVLS-2875	Application No.: 10/785,235
Information Disclosure Statement By Applicant	Applicant: Wang et al.	Group
(Use Several Sheets if Necessary)	Filing Date February 23, 2004	2812

U.S. Patent Documents

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)				Atty Docket No. NOVL085/NVLS-2875	Application No.: 10/785,235
				Applicant: Wang et al.	
				Filing Date February 23, 2004	Group 2812

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	B1	WO95/07543	03.16.95	WIPO			X	

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C1	Humayun et al., "Method for Forming Porous Films By Porogen Removal Combined With In SITU Surface Modification", Novellus Corporation, Application No. 10/404,693, filed 3/31/03, pages 1-32. Atty. Docket No. NOVLP064/NVLS-0007
	C2	Tipton et al., "Method Of Porogen Removal From Porous Low-K Films Using UV Radiation", Novellus Systems, Inc., Application No. 10/672,311, filed 9/26/03, pages 1-27. Atty. Docket No. NOVLP075/NVLS-000820
	C3	Jan, C.H., et al, <i>90NM Generation, 300mm Wafer Low k ILD/Cu Interconnect Technology</i> , 2003 IEEE Interconnect Technology Conference.
	C4	Wu et al., U.S. Application No. 10/789,103 (Atty Docket No.: NOVLP094), entitled: Methods For Producing Low-K CDO Films With Low Residual Stress
	C5	Wu et al., U.S. Application No. 10/820,525 (Atty Docket No.: NOVLP091), entitled: Methods For Producing Low-K CDO Films With Low Residual Stress
	C6	Wu et al., U.S. Application No. 10/800,409 (Atty Docket No.: NOVLP098), entitled: Methods For Producing Low-K CDO Films
	C7	U.S. Patent Application No. 10/016,017, File Date: December 12, 2001 (Atty Dkt: NOVLP030)
	C8	U.S. Patent Application No. 10/125,614, File Date: April 18, 2002 (Atty Dkt: NOVLP028)
	C9	U.S. Patent Application No. 10/202,987, File Date: July 23, 2002 (Atty Dkt: NOVLP028X1)
	C10	Tipton et al., "Method for Removal of Porogens From Porous Low-K Films Using Supercritical Fluids", Novellus Systems, Inc., Application No. 10/672,305, filed 9/26/03, pages 1-32. Atty. Docket No. NOVLP069/NVLS-000821
	C11	Cho et al., "Method and Apparatus for UV Exposure of Low Dielectric Constant Materials for Porogen Removal and Improved Mechanical Properties", Novellus Systems, Inc., Application No. 10/800,377, filed 3/11/04, pages 1-31. Atty. Docket No. NOVLP089/NVLS-2887
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Other Documents

C12	Wu et al., "Method and Apparatus of UV Exposure of Low Dielectric Constant Materials for Porogen Removal and Improved Mechanical Properties", Novellus Systems, Inc., Application No. 10/807,680, filed 3/23/04, pages 1-34. Atty. Docket No. NOVLP097/NVLS-2906
C13	Tipton et al., "Method Of Porogen Removal From Porous Low-K Films Using UV Radiation", U.S. Application No. 10/672,311, filed September 26, 2003, Office Action dated September 7, 2004 (Atty Dkt: NOVLP075/NVLS-000820)
C14	Tipton et al., "Method Of Porogen Removal From Porous Low-K Films Using UV Radiation", U.S. Application No. 10/672,311, filed September 26, 2003, Office Action dated December 28, 2004 (Atty Dkt: NOVLP075/NVLS-000820)
C15	Bandyopadhyay et al., "Method to Improve Mechanical Strength of Low-K Dielectric Film Using Modulated UV Exposure", U.S. Patent Application No. 10/825,888, filed April 16, 2004 (Atty Dkt: NOVLP088US/NVLS-2882)
C16	R.D. Miller et al., "Phase-Separated Inorganic-Organic Hybrids for Microelectronic Applications," MRS Bulletin, October 1997, Pages 44-48
C17	Jin et al., "Nanoporous Silica as an Ultralow- <i>k</i> Dielectric," MRS Bulletin, October 1997, Pages 39-42
C18	Asoh et al., "Fabrication of Ideally Ordered Anodic Porous Alumina with 63 nm Hole Periodicity Using Sulfuric Acid," J. Vac. Sci. Technol. B 19(2), Mar/Apr 2001, Pages 569-572
C19	Asoh et al., "Conditions for Fabrication of Ideally Ordered Anodic Porous Alumina Using Pretextured Al," Journal of the Electrochemica Society, 148 (4) B152-B156 (2001) Pages B152-B156
C20	Holland et al., "Nonlithographic Technique for the Production of Large Area High Density Gridded Field Sources," J. Vac. Sci. Technol. B 17(2), Mar/Apr. 1999, Pages 580-582
C21	Masuda et al. "Highly Ordered Nanochannel-Array Architecture in Anodic Alumina," App. Phys. Lett. 71(19), November 1997, Pages 2770-2772
C22	Clube et al., "White Paper from Holotronic Technologies SA; downloaded from www.hdotronic.com/whitepaper/fine-patt.pdf on March 12, 2002
C23	Meli et al., "Self-Assembled Masks for the Transfer of Nanometer-Scale Patterns into Surfaces: Characterization by AFM and LFM", Nano Letters, Vol. 2, No. 2, 2002, 131-135
C24	"Shipley Claims Porous Low K Dielectric Breakthrough," Press Release March 17, 2003.
C25	Jeffrey M. Calvert and Michael K. Gallagher, Semiconductor International, 26 (12), 56 (2003).
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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C26	Van Bavel et al., Future Fab International, 16, (2004).
	C27	Caluwaerts et al, "Post Patterning Meso Porosity Creation: A Potential Solution For Pore Sealing," IITC 2003.
	C28	Peter Singer, "New Materials and Designs to Improve Transistor Performance", April 1, 2004, Semiconductor International.
	C29	Ghani et al, "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors", IEEE, © 2003.
	C30	Bhadri N. Varadarajan, "Tensile Silicon Nitride – P1264 NESL", C & F Study, August 21, 2003.
	C31	Varadarajan, et al., "Strained Transistor Architecture and Method", Novellus Systems, Inc., Appln No. 10/923,259, filed August 20,2004, pages 1-24. [Atty Docket No. NOVLP108/NVLS-2933].
	C32	Niu et al., "Methods For Improving The Cracking Resistance Of Low-K Dielectric Materials", U.S. Application No. 10/860,340, filed June 2, 2004, (Atty Dkt: NOVLP099)
	C33	Niu et al., "Methods For Improving The Cracking Resistance Of Low-K Dielectric Materials", U.S. Application No. 10/860,340, Office Action dated March 2, 2005, (Atty Dkt: NOVLP099)
	C34	Niu et al., "Methods For Improving The Cracking Resistance Of Low-K Dielectric Materials", U.S. Application No. 10/860,340, Final Office Action dated June 13, 2005, (Atty Dkt: NOVLP099)
	C35	Varadarajan et al., "Tensile Dielectric Films Using UV Curing", U.S. Application No. 10/972,084, filed October 22, 2004 (Atty Dkt: NOVLP122)
	C36	Fox et al., "Method For Improving Mechanical Properties Of Low Dielectric Constant Materials", U.S. Application No. 10/849,568, filed May 18, 2004 (Atty Dkt: NOVLP083)
	C37	Fox et al., "Methods For Producing Low-Stress Carbon-Doped Oxide Films With Improved Integration Properties", U.S. Application No. 10/987,208, filed November 12, 2004 (Atty Dkt: NOVLP104)
	C38	Van Den Hoek et al., "VLSI Fabrication Processes For Introducing Pores Into Dielectric Materials," U.S. Application No. 11/050,621, filed January 31, 2005 (Atty Dkt: NOVLP100)
	C39	Draeger et al., "Creation Of Porosity In Low-K Films By Photo-Disassociation Of Imbedded Nanoparticles," U.S. Application No. 11/146,456, filed June 6, 2005 (Atty Dkt: NOVLP100X1)
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